S1F81150 Series

System Power Supply IC

■ DESCRIPTION

The S1F81150 is a System Power Supply IC. From the Li-Ion/Li-polymer battery, 6 channels of output voltage are generated via external devices. The 6 channels are independent of each other.
On this series, an I^2C controller (for the slave function), input and output voltage detecting functions and many kinds of operation modes (Normal, Sleep, Deep Sleep, Ultra-Energy-Saving) are provided as well as three PWM controller channels and three series regulator channel.

Table.1 Product list

Model	Package	Mask Option		
		[No.1] CH-2	[No.2] CH-3	[others]
S1F81150F0A2000	QFP12-48	2.9V	1.8V	—
S1F81150F5A2000	QFN7-48	2.9V	1.8V	(Under Development)

■ FEATURES

The features of the S1F81150 include the following:

Input voltage: V_{IN} 2.9V to 4.5V
Regulator: 6 channels

CH-1 (V_{CC1}): PWM controller

Fast synchronized rectification type PWM controller
(Connected to an external component to configure a switching regulator.)
Features include a fast response circuit using a current/voltage returning system, a short-circuit-proof circuit, a soft-start system, more compact external components by a fast clock, and dynamic voltage management system.

Output voltage: 1.5/1.4/1.3/1.2/1.1/1.0/0.9/0.85/0.8V
One of these values is to be selected via the I^2C controller.
Accuracy: within ±5%

Output current: In the sleep status: OFF.
In the normal operation: Max.: 500mA

CH-2 (V_{CC2}): PWM controller

Fast synchronized rectification type PWM controller
(Connected to an external component to configure a switching regulator.)
Features include a fast response circuit using a current/voltage returning system, a short-circuit-proof circuit, a soft-start system and more compact external components by a fast clock.

Output voltage: 2.9V (*) (*) Output voltage can be selected by metal option
Accuracy: within ±5%

Output current: In the deep sleep status: OFF.
In the backup operation: Max.: 10mA
In the normal operation: Max.: 1A

CH-3 (V_{CC3}): PWM controller

Fast synchronized rectification type PWM controller
(Connected to an external component to configure a switching regulator.)
Features include a fast response circuit using a current/voltage returning system, a short-circuit-proof circuit, a soft-start system and more compact external components by a fast clock.

Output voltage: 1.8V (*) (*) Output voltage can be selected by metal option
Accuracy: within ±5%

Output current: In the deep sleep status: OFF.
In the backup operation: Max.: 10mA
In the normal operation: Max.: 1A

CH-4 (V_{CC4}): Series regulator

A low power consumption type Series Regulator.

Output voltage:	1.3V	
Output current:	In the sleep status:	OFF.
	In the normal operation:	Max: 30mA

CH-5 (V_{CC5}): Series regulator

A low power consumption type Series Regulator.

Output voltage:	1.1V	
Output current:	In the sleep status:	OFF.
	In the normal operation:	Max: 30mA

CH-B (V_{CCB}): Series regulator

A low power consumption type Series Regulator.

Output voltage:	3.0V (±25%)	
Output current:	In the CH-2:OFF status:	Max.: 5mA
	In the normal operation:	OFF.

Conversion Efficiency:	Switching regulator (CH-1):	Max. 85% or more
	Switching regulator (CH-2/CH-3):	Max. 90% or more
Current consumption:	Ultra-Energy-Saving mode:	0.6μA (Typ. @V_{IN}=3.6V)
	Deep Sleep mode	40μA (Typ. @V_{IN}=3.6V)
	Sleep mode	85μA (Typ. @V_{IN}=3.6V)
	Normal mode	1.2mA (Typ. @V_{IN}=3.6V)
External interface:	Built-in interfaces in the I^2C controller (SDA and SCL, for the slave function only).	
Output voltage detecting function:	1 channel	(nV_{CC}_FLT)
Input voltage detecting function:	1 channel	(nBAT_FLT)
Resetting function:	1 channel	(XRST(I), nRESET(O))
Sleep function:	2 channel	(PWR_EN, SYS_EN)
DVM function:	CH-1 voltage shifting slew rate setting via I^2C controller. $\Delta V/\Delta t$ in Fig.1 can be set by register.	

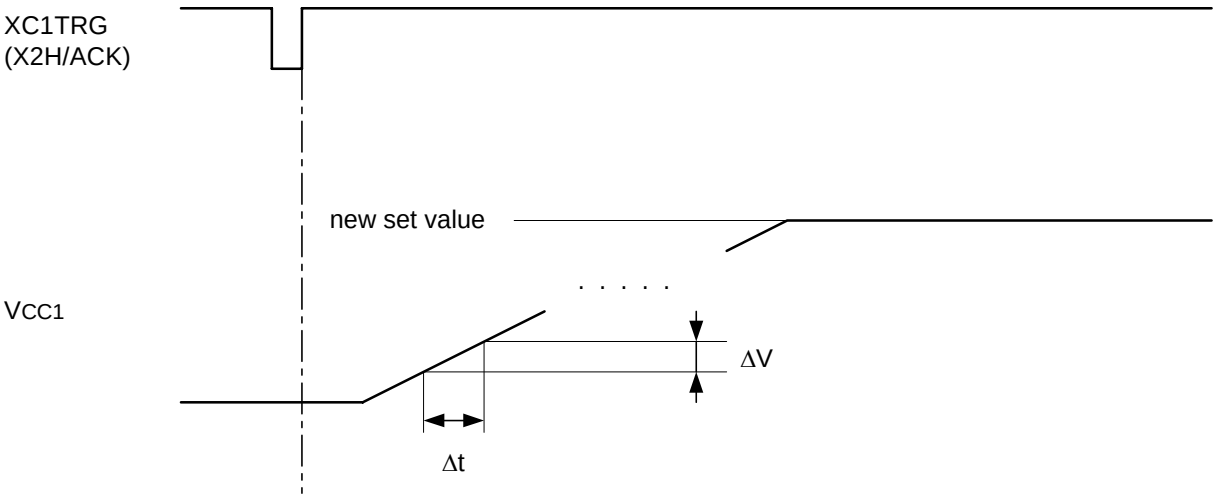

Fig.1 DVM function

■ BLOCK DIAGRAM

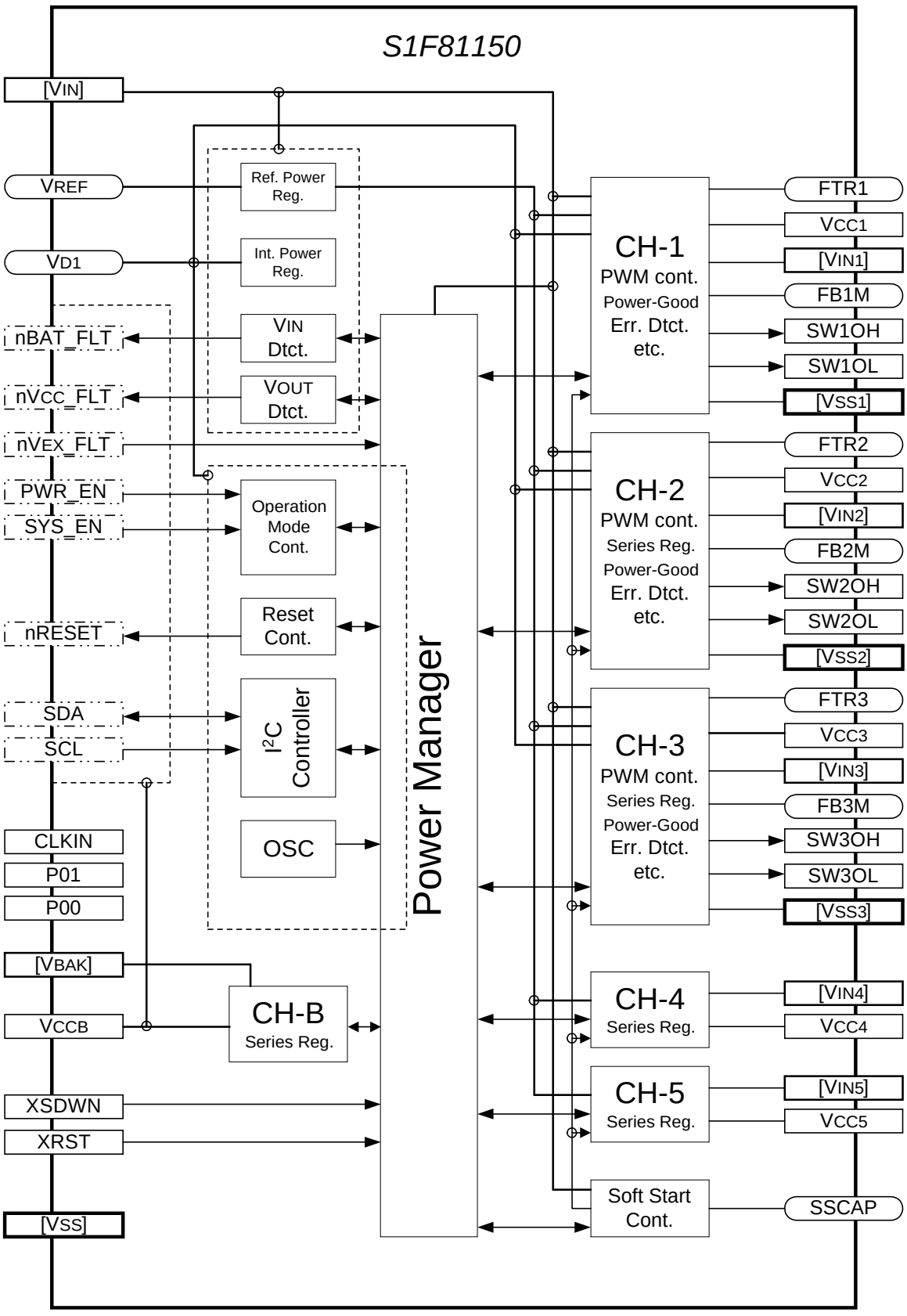

Fig.2 S1F81150 Block diagram

■ PIN ASSIGNMENT

[QFP12-48]

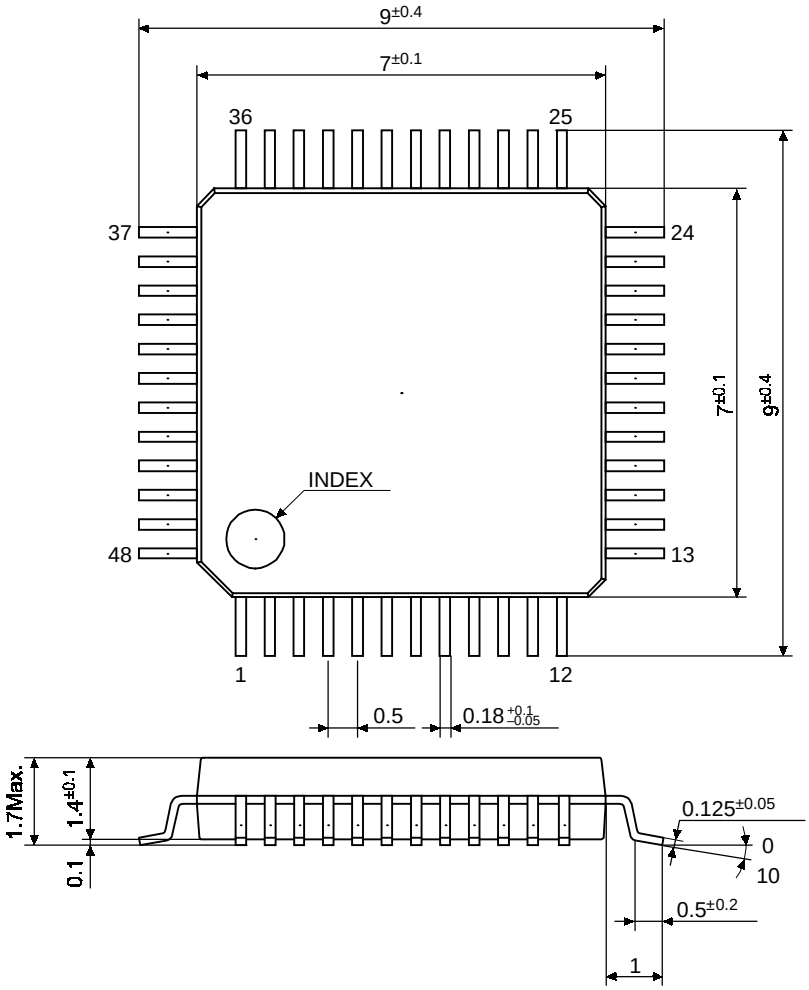

Fig.3 QFP12-48 package gram

Table 2 QFP12-48 pin assignment

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	SW3OH	13	V_{CC5}	25	V_{BAK}	37	P01
2	FB3M	14	V_{CC4}	26	V_{CCB}	38	P02
3	SW3OL	15	V_{IN4}	27	PWR_EN	39	FTR2
4	V_{SS3}	16	V_{IN5}	28	WUP	40	V_{CC2}
5	FTR1	17	XRST	29	nRESET	41	V_{IN2}
6	V_{CC1}	18	V_{IN}	30	nBAT_FLT	42	SW2OH
7	V_{IN1}	19	V_{REF}	31	nV_{CC}_FLT	43	FB2M
8	SW1OH	20	V_{D1}	32	nV_{EX}_FLT	44	SW2OL
9	FB1M	21	V_{SS}	33	SYS_EN	45	V_{SS2}
10	SW1OL	22	XSDWN	34	SCL	46	FTR3
11	V_{SS1}	23	XTEST0	35	SDA	47	V_{CC3}
12	SSCAP	24	CLKIN	36	P00	48	V_{IN3}

[QFP7-48]

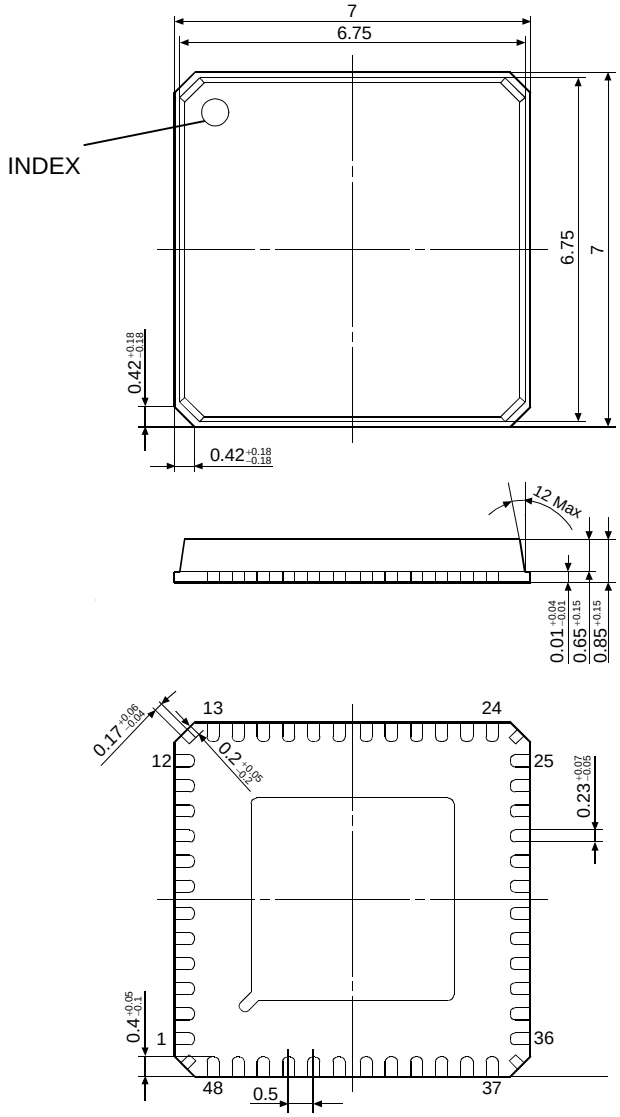

Fig.4 QFP7-48 package gram

Table.3 QFP7-48 pin assignment

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	SW3OH	13	V_{CC5}	25	V_{BAK}	37	P01
2	FB3M	14	V_{CC4}	26	V_{CCB}	38	P02
3	SW3OL	15	V_{IN4}	27	PWR_EN	39	FTR2
4	V_{SS3}	16	V_{IN5}	28	WUP	40	V_{CC2}
5	FTR1	17	XRST	29	nRESET	41	V_{IN2}
6	V_{CC1}	18	V_{IN}	30	nBAT_FLT	42	SW2OH
7	V_{IN1}	19	V_{REF}	31	nV_{CC}_FLT	43	FB2M
8	SW1OH	20	V_{D1}	32	nV_{EX}_FLT	44	SW2OL
9	FB1M	21	V_{SS}	33	SYS_EN	45	V_{SS2}
10	SW1OL	22	XSDWN	34	SCL	46	FTR3
11	V_{SS1}	23	XTEST0	35	SDA	47	V_{CC3}
12	SSCAP	24	CLKIN	36	P00	48	V_{IN3}

■ PIN DESCRIPTION

Table.3 S1F81150 Pin description

No.	Name	I/O	Function	Level	Pin No.
[Power terminal/control terminal]					
1	V_{IN}	Power	Main power (+) input terminal	—	
2	V_{SS}	Power	Main power (-) input terminal	—	
3	V_{D1}	Analog	Internal constant power output terminal	—	
4	V_{REF}	Analog	Reference power output terminal	—	
5	nVCC_FLT	O	Output detection result output terminal	V_{CCB}	
6	nBAT_FLT	O	Input detection result output terminal	V_{CCB}	
7	nRESET	O	System reset output terminal	V_{CCB}	
8	PWR_EN	I	Mode setting input terminal	V_{CCB}	
9	SYS_EN	I	Mode setting input terminal	V_{CCB}	
10	WUP	O	V_{CC1} power change indiction output terminal	V_{CCB}	
11	nVEX_FLT	I	External power detection result input terminal	V_{CCB}	
12	CLKIN	I	External clock input terminal	V_{CC2}	
13	XRST	I	Reset input terminal	V_{IN}	
14	XTEST0	I	Test terminal	V_{IN}	
15	XSDWN	I	Ultra-energy-saving mode setting terminal	V_{IN}	
16	P00	I/O	General purpose I/O terminal	V_{CC2}	
17	P01	I/O	General purpose I/O terminal	V_{CC2}	
18	P02	I/O	Test terminal	V_{CC2}	
19	SCL	I	I^2C clock input terminal	V_{CCB}	
20	SDA	I/O	I^2C data input/output terminal	V_{CCB}	
21	SSCAP	Analog	Soft start setting terminal	—	
[CH-1 related terminal]					
22	V_{IN1}	Power	Main power (+) input terminal	—	
23	SW1OH	O	P-ch power MOS drive output terminal	V_{IN1}	
24	SW1OL	O	N-ch power MOS drive output terminal	V_{IN1}	
25	FB1M	Analog	Output current feed back input terminal	—	
26	V_{CC1}	Analog	Output power feed back input terminal	—	
27	FTR1	Analog	N.C.	—	
28	V_{SS1}	Power	Main power (-) input terminal	—	
[CH-2 related terminal]					
29	V_{IN2}	Power	Main power (+) input terminal	—	
30	SW2OH	O	P-ch power MOS drive output terminal	V_{IN2}	
31	SW2OL	O	N-ch power MOS drive output terminal	V_{IN2}	
32	FB2M	Analog	Output current feed back input terminal	—	
33	V_{CC2}	Analog	Output power feed back input terminal	—	
34	FTR2	Analog	Analog filter terminal	—	
35	V_{SS2}	Power	Main power (-) input terminal	—	
[CH-3 related terminal]					
36	V_{IN3}	Power	Main power (+) input terminal	—	
37	SW3OH	O	P-ch power MOS drive output terminal	V_{IN3}	
38	SW3OL	O	N-ch power MOS drive output terminal	V_{IN3}	
39	FB3M	Analog	Output current feed back input terminal	—	
40	V_{CC3}	Analog	Output power feed back input terminal	—	
41	FTR3	Analog	Analog filter terminal	—	
42	V_{SS3}	Power	Main power (-) input terminal	—	
[CH-4 related terminal]					
43	V_{IN4}	Power	CH-4 regulator power (+) input terminal	—	
44	V_{CC4}	Analog	V_{CC4} power output terminal	—	
[CH-5 related terminal]					
45	V_{IN5}	Power	CH-5 regulator power (+) input terminal	—	
46	V_{CC5}	Analog	V_{CC5} power output terminal	—	
[CH-B related terminal]					
47	V_{BAK}	Power	CH-B regulator power (+) input terminal	—	
48	V_{CCB}	Analog	V_{CCB} power output terminal	—	

■ EXTERNAL CONNECTION DIAGRAM

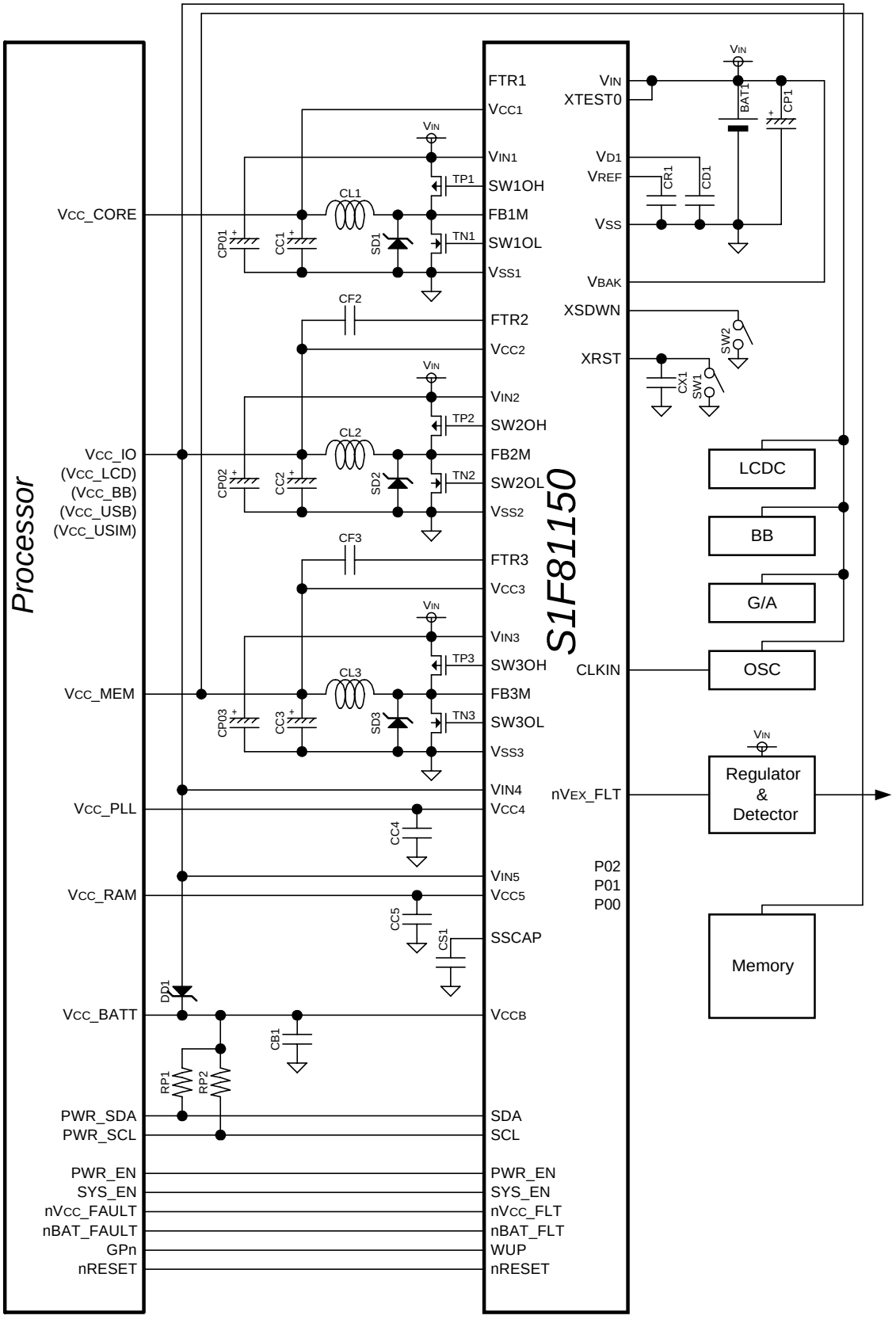

Fig.5 S1F81150 external connection diagram

S1F81150 Series

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